DATA SHEET

NEC

# MOS FIELD EFFECT POWER TRANSISTOR
# 2SK1992/2SK1993

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The 2SK1992/2SK1993 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

### FEATURES

- Low On-state Resistance
  $R_{DS(on)} \leqq 0.9/1.0\ \Omega$ ($V_{GS}$ = 10 V, $I_D$ = 3.0 A)
- Low $C_{iss}$ $C_{iss}$ = 1 060 pF TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

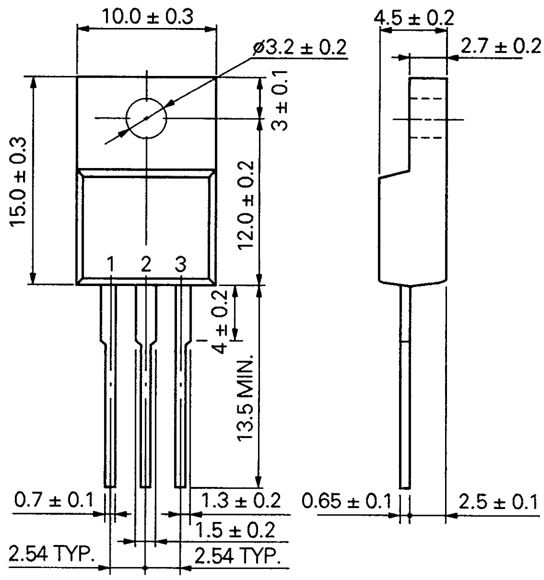
### ABSOLUTE MAXIMUM RATINGS ($T_a$ = 25 °C)

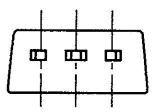
| | | | |
|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | 450/500 | V |
| Gate to Source Voltage | $V_{GSS}$ | ±30 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ±6.0 | A |
| Drain Current (pulse) | $I_{D(pulse)}$* | ±24 | A |
| Total Power Dissipation ($T_c$ = 25 °C) | $P_{T1}$ | 35 | W |
| Total Power Dissipation ($T_a$ = 25 °C) | $P_{T2}$ | 2.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| Single Avalanche Current | $I_{AS}$** | 9.0 | A |
| Single Avalanche Energy | $E_{AS}$** | 243 | mJ |

* PW ≦ 10 $\mu$s, Duty Cycle ≦ 1 %

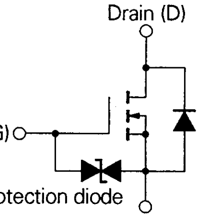
** Starting $T_{ch}$ = 25 °C, $R_G$ = 25 Ω, $V_{GS}$ = 20 V → 0

### PACKAGE DIMENSIONS
(in millimeters)



1. Gate
2. Drain
3. Source

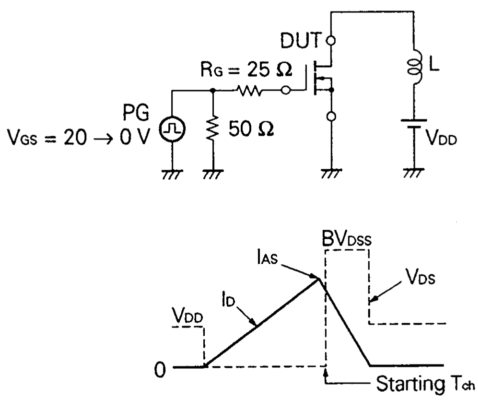



Document No. TC–2451
(O.D. No. TC–7914)
Date Published August 1993 M
Printed in Japan

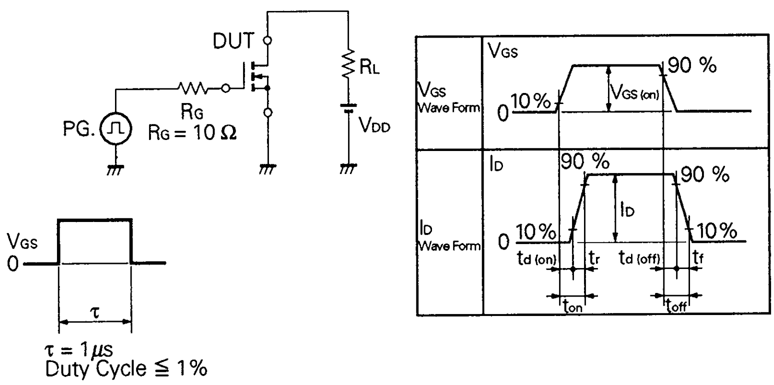
## ELECTRICAL CHARACTERISTICS ($T_a$ = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance (2SK1992) | $R_{DS(on)}$ | | 0.7 | 0.9 | Ω | $V_{GS}$ = 10 V, $I_D$ = 3.0 A |
| Drain to Source On-state Resistance (2SK1993) | | | 0.8 | 1.0 | Ω | $V_{GS}$ = 10 V, $I_D$ = 3.0 A |
| Gate to Source Cutoff Voltage | $V_{GS(off)}$ | 2.5 | | 3.5 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA |
| Forward Transfer Admittance | $\|y_{fs}\|$ | 2.8 | | | S | $V_{DS}$ = 10 V, $I_D$ = 3.0 A |
| Drain Leakage Current (2SK1992/1993) | $I_{DSS}$ | | | 100 | μA | $V_{DS}$ = 450/500 V, $V_{GS}$ = 0 |
| Gate to Source Leakage Current | $I_{GSS}$ | | | ±10 | μA | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 |
| Input Capacitance | $C_{iss}$ | | 1 060 | | pF | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz |
| Output Capacitance | $C_{oss}$ | | 340 | | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 150 | | pF | |
| Turn-On Delay Time | $t_{d(on)}$ | | 20 | | ns | $V_{GS}$ = 10 V, $V_{DD}$ = 150 V, $I_D$ = 3.0 A, $R_G$ = 10 Ω, $R_L$ = 50 Ω |
| Rise Time | $t_r$ | | 30 | | ns | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 70 | | ns | |
| Fall Time | $t_f$ | | 20 | | ns | |
| Total Gate Charge | $Q_G$ | | 36 | | nC | $V_{GS}$ = 10 V, $I_D$ = 6 A, $V_{DD}$ = 400 V |
| Gate to Source Charge | $Q_{GS}$ | | 7 | | nC | |
| Gate to Drain Charge | $Q_{GD}$ | | 21 | | nC | |
| Diode Forward Voltage | $V_{F(S-D)}$ | | 0.9 | | V | $I_F$ = 6 A, $V_{GS}$ = 0 |
| Reverse Recovery Time | $t_{rr}$ | | 420 | | ns | $I_F$ = 6 A, di/dt = 50 A/μs |
| Reverse Recovery Charge | $Q_{rr}$ | | 2.0 | | μC | |

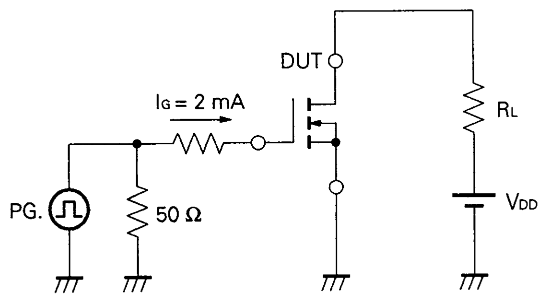
### Test Circuit 1: Avalanche Capability



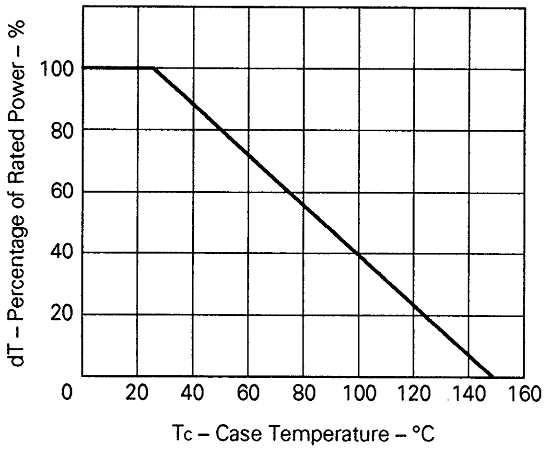

### Test Circuit 2: Switching Time

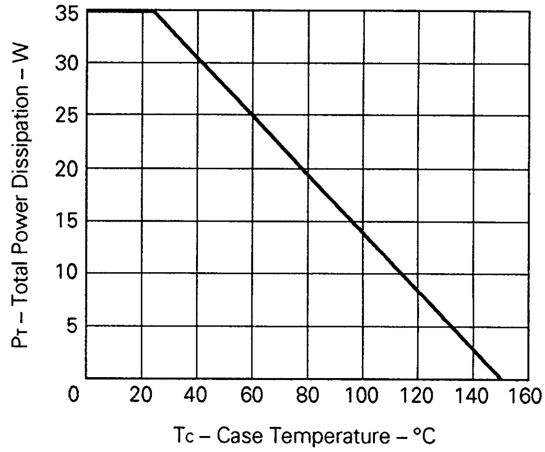


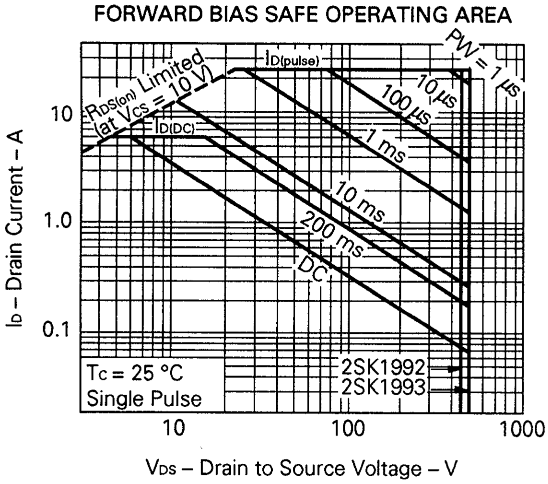

### Test Circuit 3: Gate Charge

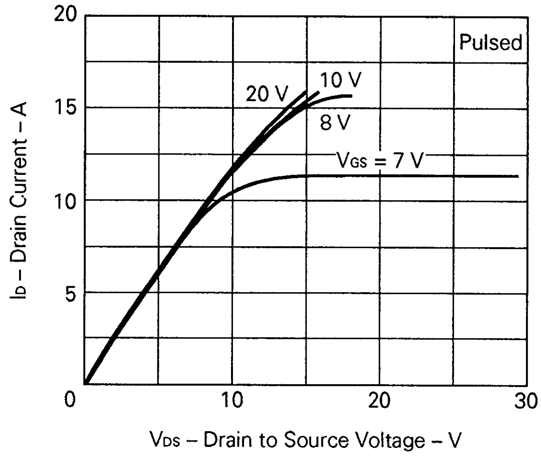


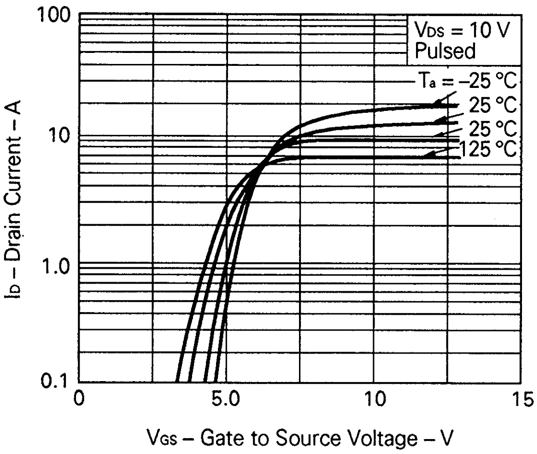
## TYPICAL CHARACTERISTICS (Ta = 25 °C)



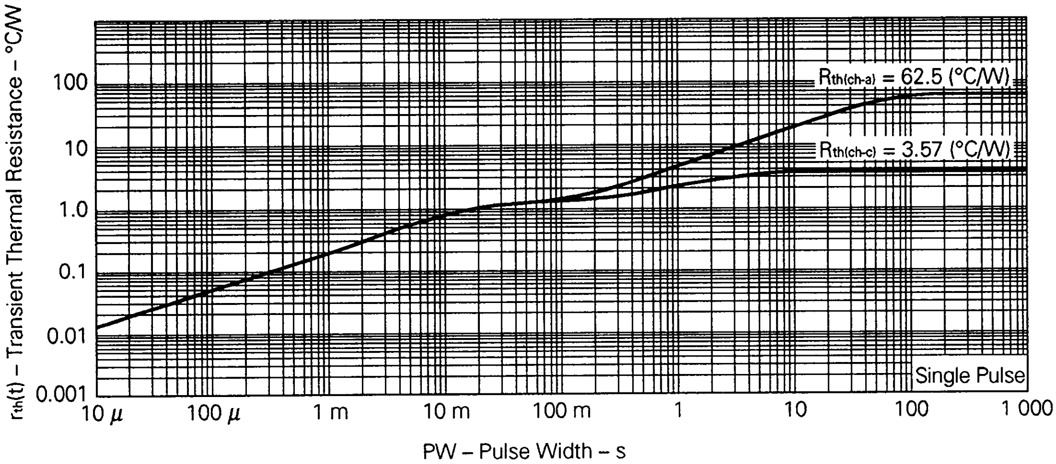



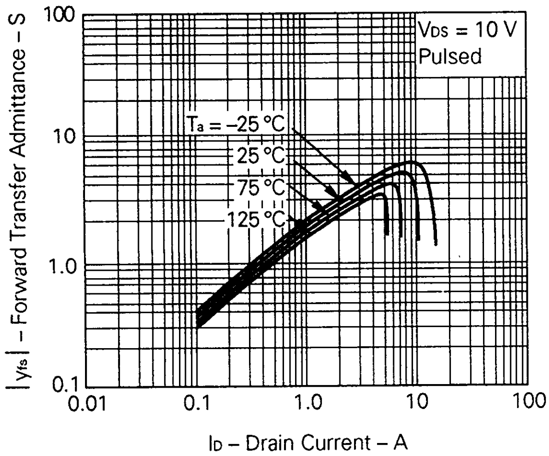



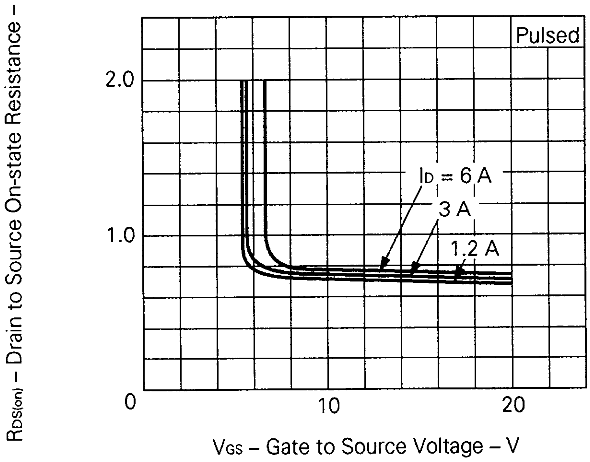
### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



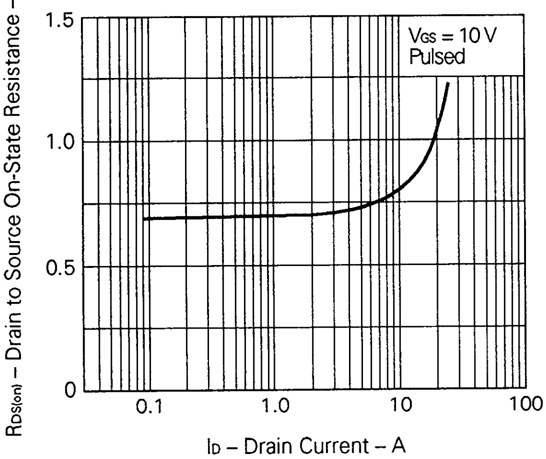

### FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



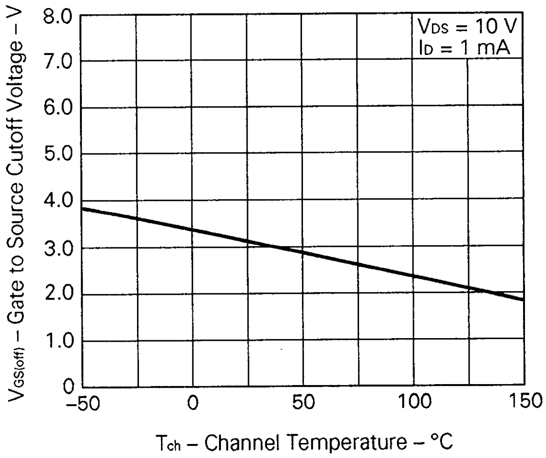

### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



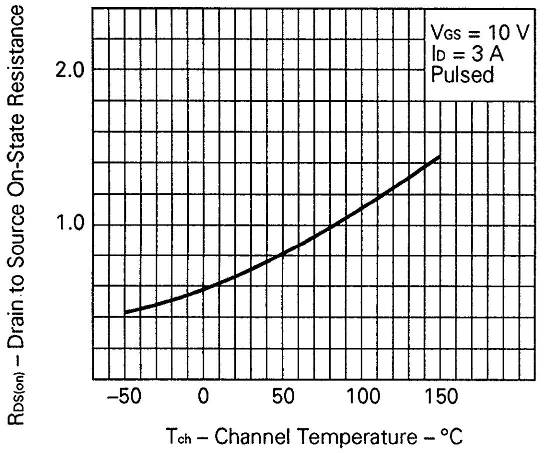

### DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



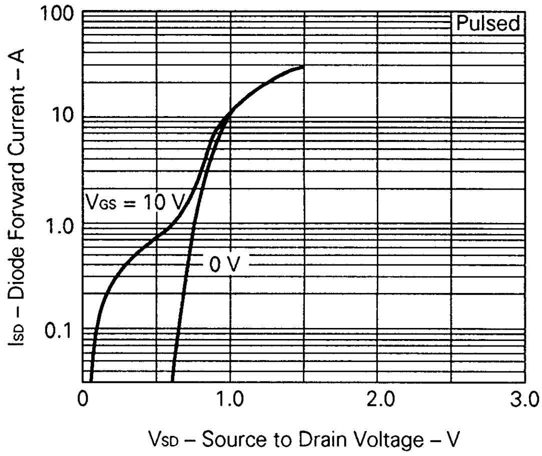

### GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



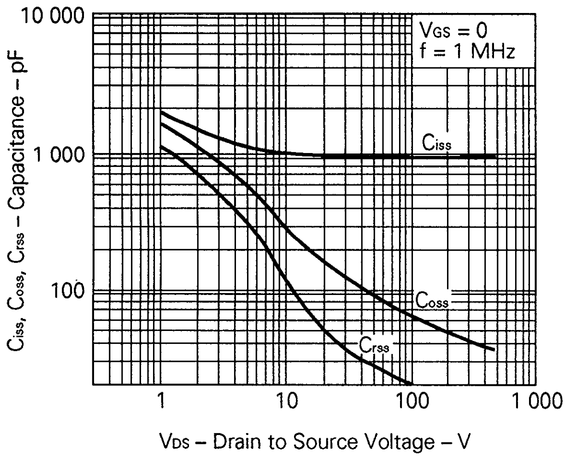
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



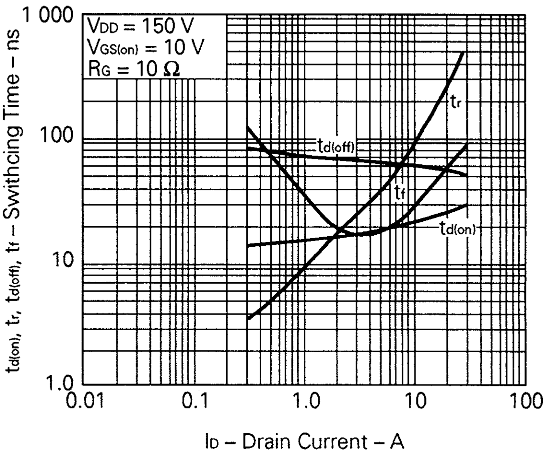

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



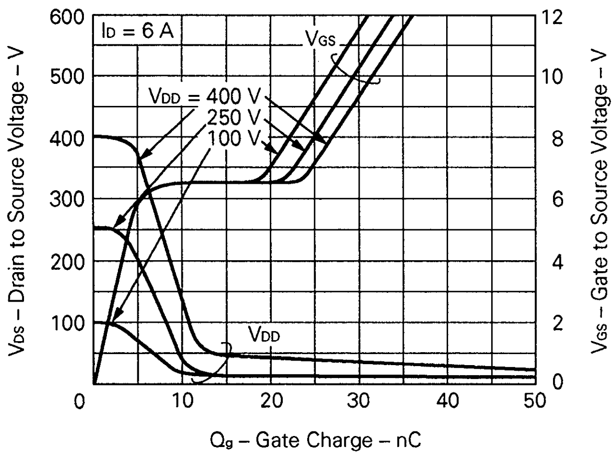

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



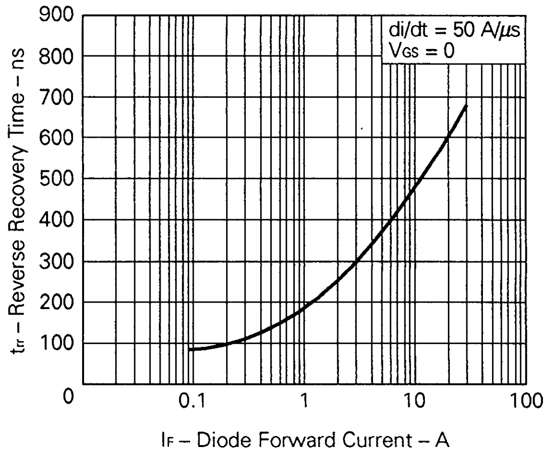

SWITCHING CHARACTERISTICS



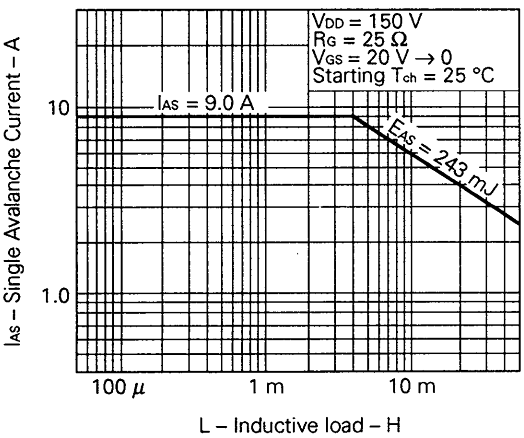

DYNAMIC INPUT CHARACTERISTICS



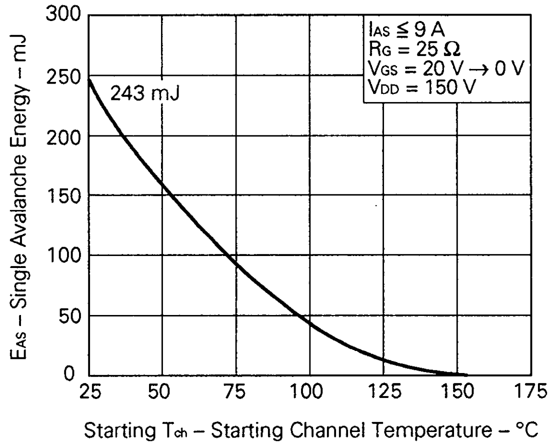

REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD




SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



**Reference**

| Application note name | No. |
|---|---|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

[MEMO]